Claims

What is claimed is:

1. An image-processing device, comprising:

a solid-state image-pick up device provided with a plurality of unit pixels arranged in a matrix, each unit pixel including a photo diode and a transistor for detecting a light signal;

a signal-processing unit that processes an output signal from the solid-state image-pick up device and outputs the processed signal as an image signal; and

an output circuit arranged in the solid-state image-pick up device that outputs a valid signal to the signal-processing unit, the valid signal indicating whether the output of signal-processing unit is valid or not in response to an operation of the solid-state image-pick up device.

2. An image-processing device according to claim 1 wherein the solid-state image-pick up device further comprises a MOS solid-state image-pick up device with a threshold voltage modulation system.

3. An image-processing device, comprising:

a solid-state image-pick up device provided with a plurality of unit pixels arranged in a matrix, each unit pixel including a photo diode and a transistor for detecting a light signal;

a signal-processing unit that processes an output signal from the solid-state image-pick up device and outputs the processed signal as an image signal; and

an output circuit, arranged in the solid-state image-pick up device, that outputs a valid signal to the signal-processing unit, the valid signal controlling whether the signal-processing unit performs the signal processing operation or not in response to an operation of the solid-state image-pick up device.

4. An image-processing device according to claim 3 wherein the solid-state image-pick up device further comprises a MOS solid-state image-pick up device with a threshold voltage modulation system.

5. An image-processing device according to claim 1, wherein the output circuit outputting the valid signal makes the valid signal deactivated at a time when at least one of an idle frame, an accumulation frame, an interlacing frame and an H blanking period is activated.

6. An image-processing device according to claim 5, wherein the H blanking period makes the H blanking operation deactivated during the H blanking period in the accumulation state, if the accumulation state where electric charges are stored in the solid-state image-processing device continues for more than one frame.

7. An image-processing device according to claim 1, wherein the output circuit outputting the valid signal makes the valid signal deactivated at a time when at least one of an idle frame, an accumulation frame, an interlacing frame, an H blanking period and a period for indicating a final line counted value is activated.

8. An image-processing device according to claim 7, wherein the H blanking period makes the H blanking operation deactivated during the H blanking period in the accumulation state, if the accumulation state where electric charges are stored in the solid-state image-processing device continues for more than one frame.

9. An image-processing device according to claim 1, wherein the output circuit outputting the valid signal makes the valid signal activated at s time when all of an idle frame, an accumulation frame, an interlacing frame, an H blanking period and a period for indicating a final line counted value are deactivated and a period for reading out an image signal from a line memory is activated.

10. An image-processing device according to claim 9, wherein the H blanking period makes the H blanking operation deactivated during the H blanking period in the accumulation state, if the accumulation state where electric charges are stored in the solid-state image-processing device continues for more than one frame.

11. An image-processing device according to claim 1, wherein the output circuit outputting the valid signal makes:

the valid signal deactivated if image data is different from setting conditions; and

the valid signal activated if image data is the same as the setting conditions,

under conditions when the solid-state image-processing device always outputs normal image data.

12. An image-processing device according to claim 11, wherein image data that is different from the setting conditions is image data where the conditions including any of a frame rate, a shutter speed and a scanning direction are changed.

13. An image-processing device according to claim 1, wherein the output circuit outputting the valid signal increases a deactivated rate of the valid signal intermittently as a frame unit in response to a decreasing frame rate when the solid-state image-processing device is operated with a low frame rate.

14. A method of processing an image-processing device including a solid-state image-pick up device provided with a plurality of unit pixels arranged in a matrix, each unit pixel including a photo diode and a transistor for detecting a light signal and a signal-processing unit that processes an output signal from the solid-state image-pick up device, the method comprising:

a step of outputting a valid signal to the signal-processing unit processing from the solid-state image-pick up device, the valid signal indicating whether the output of signal-processing unit is valid or not in response to an operation of the solid-state image-pick up device.

15. A method of processing an image-processing device according to claim 12 wherein the solid-state image-pick up device further comprises a MOS solid-state image-pick up device with a threshold voltage modulation system.

16. An image-processing device according to claim 3, wherein the output circuit outputting the valid signal makes the valid signal deactivated at a time when at least one of an idle frame, an accumulation frame, an interlacing frame and an H blanking period is activated.

17. An image-processing device according to claim 16, wherein the H blanking period makes the H blanking operation deactivated during the H blanking period in the accumulation state, if the accumulation state where electric charges are stored in the solid-state image-processing device continues for more than one frame.

18. An image-processing device according to claim 3, wherein the output circuit outputting the valid signal makes the valid signal deactivated at a time when at least one of an idle frame, an accumulation frame, an interlacing frame, an H blanking period and a period for indicating a final line counted value is activated.

19. An image-processing device according to claim 18, wherein the H blanking period makes the H blanking operation deactivated during the H blanking period in the accumulation state, if the accumulation state where electric charges are stored in the solid-state image-processing device continues for more than one frame.

20. An image-processing device according to claim 3, wherein the output circuit outputting the valid signal makes the valid signal activated at s time when all of an idle frame, an accumulation frame, an interlacing frame, an H blanking period and a period for indicating a final line counted value are deactivated and a period for reading out an image signal from a line memory is activated.

21. An image-processing device according to claim 20, wherein the H blanking period makes the H blanking operation deactivated during the H blanking period in the accumulation state, if the accumulation state where electric charges are stored in the solid-state image-processing device continues for more than one frame.

22. An image-processing device according to claim 3, wherein the output circuit outputting the valid signal makes:

the valid signal deactivated if image data is different from setting conditions; and

the valid signal activated if image data is the same as the setting conditions,

under conditions when the solid-state image-processing device always outputs normal image data.

23. An image-processing device according to claim 22, wherein image data that is different from the setting conditions is image data where the conditions including any of a frame rate, a shutter speed and a scanning direction are changed.

24. An image-processing device according to claim 3, wherein the output circuit outputting the valid signal increases a deactivated rate of the valid signal intermittently as a frame unit in response to a decreasing frame rate when the solid-state image-processing device is operated with a low frame rate.